I CLAIM:

1. Apparatus for processing data, said apparatus comprising:

an instruction fetching circuit operable to fetch program instructions from a sequence of memory locations;

an instruction decoder responsive to program instructions fetched by said instruction fetching circuit to control data processing operations specified by said program instructions; and

an execution circuit operable under control of said instruction decoder to execute said data processing operations; wherein

said instruction decoder is responsive to an execute block instruction to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction.

2. Apparatus as claimed in claim 1, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

3. Apparatus as claimed in any one of claims 1 and 2, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

4. Apparatus as claimed in any one of claims 1, 2 and 3, wherein said location field is an offset field specifying said location of said block of two or more program

instructions relative to a memory location of said execute block instruction.

5. Apparatus as claimed in any one of the preceding claims, comprising a program counter register operable to store an address indicative of a memory location of a program instruction being executed within said sequence of program instructions.

6. Apparatus as claimed in any one of the preceding claims, comprising a block counter register operable to store a block count value indicative of a location of a program instruction being executed within said block of two or more program instructions.

7. Apparatus as claimed in claims 5 and 6, wherein when executing said block of two or more program instructions, said program counter registers stores an address indicative of a memory location of said execute block instruction and said block counter register stores a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction.

8. Apparatus as claimed in any one of claims 6 and 7, comprising an exception handling circuit operable upon occurrence of an exception during execution of said block of two or more instructions to store said block count value and upon completion of handling of said exception to restart execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

9. Apparatus as claimed in claims 6 and 8, wherein said exception handling circuit is operable to store said address of said execute block instruction upon occurrence of said exception and to restore said address of said execute block instruction to said program counter register upon said completion of handling of said

exception.

10. Apparatus as claimed in claims 2 and 5, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.

11. A method for processing data, said method comprising the steps of:

fetching program instructions from a sequence of memory locations with an instruction fetching circuit;

controlling data processing operations specified by said program instructions with an instruction decoder; and

executing said data processing operations with an execution circuit controlled by said instruction decoder; wherein

said instruction decoder is responsive to an execute block instruction to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction.

12. A method as claimed in claim 11, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

13. A method as claimed in any one of claims 11 and 12, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

14. A method as claimed in any one of claims 11, 12 and 13, wherein said location field is an offset field specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction.

15. A method as claimed in any one of claims 11 to 14, comprising storing within a program counter register an address indicative of a memory location of a program instruction being executed within said sequence of program instructions.

16. A method as claimed in any one of claims 11 to 15, comprising storing within a block counter register a block count value indicative of a location of a program instruction being executed within said block of two or more program instructions.

17. A method as claimed in claims 15 and 16, wherein when executing said block of two or more program instructions, said program counter registers stores an address indicative of a memory location of said execute block instruction and said block counter register stores a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction.

18. A method as claimed in any one of claims 16 and 17, comprising upon occurrence of an exception during execution of said block of two or more instructions storing said block count value and upon completion of handling of said exception restarting execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

19. A method as claimed in claims 15 and 18, wherein upon occurrence of said exception storing said address of said execute block instruction and restoring said

address of said execute block instruction to said program counter register upon said completion of handling of said exception.

20. A method as claimed in claims 12 and 15, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.

21. A computer program product including a computer program operable to control a data processing apparatus having an instruction fetching circuit operable to fetch program instructions from a sequence of memory locations, an instruction decoder responsive to program instructions fetched by said instruction fetching circuit to control data processing operations specified by said program instructions, and an execution circuit operable under control of said instruction decoder to execute said data processing operations; said computer program including one or more an execute block instructions operable to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction.

22. A computer program product as claimed in claim 21, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

23. A computer program product as claimed in any one of claims 21 and 22, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

24. A computer program product as claimed in any one of claims 21, 22 and 23, wherein said location field is an offset field specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction.

25. A computer program product as claimed in any one of claims 21 to 24, wherein a program counter register stores an address indicative of a memory location of a program instruction being executed within said sequence of program instructions.

26. A computer program product as claimed in any one of claims 21 to 25, wherein a block counter register stores a block count value indicative of a location of a program instruction being executed within said block of two or more program instructions.

27. A computer program product as claimed in claims 25 and 26, wherein when executing said block of two or more program instructions, said program counter registers stores an address indicative of a memory location of said execute block instruction and said block counter register stores a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction.

28. A computer program product as claimed in any one of claims 26 and 27, wherein upon occurrence of an exception during execution of said block of two or more instructions storing said block count value and upon completion of handling of said exception restarting execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

29. A computer program product as claimed in claims 25 and 28, wherein upon

occurrence of said exception storing said address of said execute block instruction and restoring said address of said execute block instruction to said program counter register upon said completion of handling of said exception.

30. A computer program product as claimed in claims 22 and 25, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.